ECE 302

ELECTRONIC CIRCUITS

FALL 2019

COURSE:	M W Th	5:50 - 6:40 pm	Room 1345 EB
PREREQ:	ECE 202		
INSTRUCTOR:	G.M. Wierzba	Room 3215 EB	355-5225; wierzba@msu.edu
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OFFICE HRS:	M W Th	4:10 - 5:00 pm	or by appointment

TEXTS: G.M. Wierzba, *ECE 302 Course e-Notes, Fall 2019 Edition,* (free for all registered students)

Schubert & Kim, *Fundamentals of Electronics*, Books 1-3, Morgan & Claypool, 2014 (Revised version of *Active and Non-Linear Electronics*, Wiley, 2004)

J. O. Attia, *PSpice and MATLAB for Electronics*, CRC Press, 2010
(M. Rashid, *Intro. To PSpice Using Orcad for Circuits and Electronics*, Pearson Prentice Hall, 2004 – out of print)

GRADING:

Three one-hour exams	(9/23, 10/21, 11/18)	200 pts
Final exam*	(Mon., Dec 9, 8 - 10 pm)	200 pts
Homework *	(normalized)	50 pts

**You must obtain a passing grade to pass the course.*

POLICIES: You are expected to arrive for class on time. No electronic devices or laptops are allowed during class. No student can wear earphones during class.

HOMEWORK: Homework is to be done on 8.5" x 11" paper using only one side. It must be stapled and ragged edges must be trimmed. Whenever possible, the correct answer is to be circled or boxed. You may work with other students (list all names below yours) but the work you submit must be done by you. Assignments which are identical will all receive a grade of **zero**. You must type and run all of your own computer work. Copying of old assignments or computer files will be dealt with severely.

OTHER: Only simple scientific calculators are allowed for exams. Exam questions may have little or no partial credit. There are NO MAKE UP EXAMS. Your lowest hourly exam grade will be dropped in computing your grade. Late homework WILL NOT be accepted. Your lowest homework grade will be dropped in computing your normalized homework grade.

An 85% attendance rate is required to pass the course, that is, you can miss 7 classes. Please keep your own record of absences.

DETAILED TOPICS:

Chapter 2: Diode Characteristics and Circuits

2.1 Basic Functional Requirements of an Ideal Diode
Piecewise Linear Model, Transition Point, Assumed States for Analysis, Strategy for Guessing States

2.2 Semiconductor Diode V-I Relationship
Physics of the P-N Junction, Shockley Equation, Approximations, Dynamic Resistance

2.3 Diode as a Circuit Element
Transcendental Equation, SPICE Model Parameters, Software Curve Tracer, Effects of Temperature

2.4 Load Lines
Graphical Solutions to Static Circuits, Inspection Short Cut, Graphical Solutions of Circuits with Time-Varying Sources

2.5 Simplified Piecewise Linear Model

2.6 Diode Applications
Positive Clipper with SPICE Evaluation, Negative Clipper with SPICE Evaluation, Double Clipper with SPICE Evaluation, Half-Wave Rectifier with SPICE Evaluation, Full-Wave Rectifier with SPICE Evaluation, Filtered Full-Wave Rectifier with SPICE Evaluation, Transformers, Peak Detectors, Clamping Circuits, Voltage Multiplier, Or-Gate, And-Gate

2.7 Zener Diode and Applications
Piecewise Linear Model, Shunt Regulator, Design - Cigarette Lighter Adapter for a CD Player, SPICE Evaluation

Chapter 3: Bipolar Junction Transistor (BJT) Characteristics

3.1 BJT V-I Relationships
NPN BJT, Physical Operation in the Active Region, Physical Operation in the Cut-Off Region, Physical Operation in the Saturation Region, Physical Operataion in the Inverse-Active Region, PNP BJT, Ebers-Moll Equations, SPICE Model Parameters, Software Curve Tracer

3.4 Modeling of the BJT in its Regions of Operation
Active, Saturation, Cut-Off, Inverse-Active, Inverse-Saturated, Inverse Cut-Off, Edge-of-Saturation, Edge-of-Cut-Off, Edge-of-Saturation Reverse, Edge-of-Cut-Off-Reverse

3.2 The BJT as a Circuit Element
Assumed States Analysis, Strategies for Guessing the State of an NPN (PNP) BJT, Load-Line Approach, Ebers-Moll Approach

3.6 Biasing the BJT
Fixed Bias Circuit, Emitter Bias Circuit with Two Supplies, Emitter Bias Circuit with One Supply, Emitter Bias Circuit Design, Biasing PNP Transistors

3.5 Digital Electronic Applications
Resistor-Transistor Logic Gates, Logic Level Diagram, Fanout, Nor-Gate, Step Response of an RL (RC) Circuit, Switching Inductive Loads, Damping Diode, SPICE Evaluation, Switching Capacitive Loads, SPICE Evaluation

Chapter 5: Single Transistor Amplifiers

- 5.2 BJT Low-Frequency Models
  Definition of Small Signal, Small-Signal Analysis Algorithm Small-Signal Model for an NPN, PNP BJT and a diode
- 5.3 Common-Emitter Amplifier
  Voltage Gain, Input Impedance, Current Gain, Power Gain, Output Impedance, SPICE Verification
- 5.4 Common-Collector (Emitter Follower) Amplifier
  Voltage Gain, Input Impedance, Current Gain, Power Gain, Output Impedance
- 5.5 Common-Base Amplifier
  Voltage Gain, Input Impedance, Current Gain, Power Gain, Output Impedance

Chapter 6: Multiple-Transistor Amplifiers

- 6.1 Using Simple Stages Cascaded
  Common-Emitter Common-Emitter Amplifier
- 6.3 Differential Pairs
  Bartlett's Bisection Theorem, Basic Differential Amplifier, Differential Gain, Common-Mode Gain, Input Resistance, Common-Mode Rejection Ratio, Current Source Biasing

Chapter 10: Frequency Response of Transistor Amplifiers

- 10.X Departure from Ideal Diode Performance
  Depletion Capacitance, Diffusion Capacitance, SPICE Parameters of a Diode, AC Model of a Diode, SPICE Testing of V-I Characteristics
- 10.Y Departure from Ideal Transistor Performance
  SPICE Parameters of a BJT, AC Model of a BJT, SPICE Testing of V-I Characteristics, Measuring Low Frequency AC Parameters, AC Model for a BJT (Giacoletto Model)
- 10.6 High-Frequency Amplifiers
  Wideband Common-Emitter Amplifier, SPICE Evaluation, Short Circuit Time Constants, Open Circuit Time Constants, Loading Effects on Bandwidth

Chapter 4: Field-Effect Transistor Characteristics

- 4.1 Junction Field-Effect Transistors (JFETs)
  N-Channel JFET, Physical Operation in Cut-Off and Ohmic Region, Physical Operation in Saturation, Character Curves and Equations, P-Channel JFET
- 4.2 Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs)
  Enhancement N-Channel MOSFET, Physical Operation in Cut-Off and Ohmic Region, Physical Operation in Saturation, Character Curves and Equations, Enhancement P-Channel MOSFET, FET - BJT Analogy

4.3 FET as a Circuit Element

JFET SPICE Model Parameters, Software Curve Tracer, MOSFET SPICE Model Parameters, Software Curve Tracer, The JFET as a Voltage-Controlled Resistance with SPICE Verification, The JFET as a Current Source with SPICE Verification

4.6 Biasing the FET

Fixed-Bias Circuit, Self-Bias Circuit, Fixed-Plus Self-Bias Circuit

4.3 FET as a Circuit Element

NMOS Inverter with a Pull-Up Resistor, NMOS Inverter with Capacitive Loads, CMOS Inverter, SPICE Transfer Curves, CMOS NOR-Gate, CMOS NAND-Gate, CMOS Transmission- Gate, Bulk-Pin Potential

5.7 FET Low-Frequency Models

Definition of Small Signal, Small-Signal Analysis Algorithm, Small-Signal Model for an N- and P- Channel JEFT, Small-Signal Model for an N- and P-Channel MOSFET

5.8 The Common-Source Amplifier

Voltage Gain, Input Impedance, Current Gain, Power Gain, Output Impedance, Comparison of a Common-Source Amplifier and a Common-Emitter Amplifier

6.1 Using Simple Stages Cascaded

Broadband Amplifier: Common-Source Common-Base Amplifier

Chapter 7: Power Amplifiers and Output Stages

7.1 Power Amplifier Classification

Class A, Total Harmonic Distortion, SPICE Measurement, Efficiency

7.3 Complementary Pair Power Booster (Class B Amplifier)

Efficiency, Distortion, SPICE Verification

7.4 Class AB Power Amplifiers

15-Watt Power Amplifier

7.6 Thermal Considerations