ECE 877 - Syllabus
ECE Cleanroom Procedures
Fall 2019
Instructor: Tim Hogan

TIME: Lecture: 3:00pm-3:50pm Mondays and Wednesdays
Laboratory: 11:30am-2:20pm Tuesdays (section 001)
3:00pm-5:50pm Thursdays (section 002)
3:00pm-5:50pm Tuesdays (section 003)

ROOM: Lecture: 1300 Engineering Building
Laboratory: C16 Engineering Research Complex (entrance is C18 ERC)

INSTRUCTOR: Tim Hogan
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OFFICE HRS: 4:00pm-5:00pm Mondays and Wednesdays, 10:00am-11:00am Thursdays in 2308A Engineering Building, **or by appointment (these should be arranged by email)**.

COURSE WEB SITE: The primary web site is via the D2L Course Management System. Please point your browser to the following URL: https://d2l.msu.edu/ and log-in with your MSUNet ID and password.

COURSE DESCRIPTION: This course is designed for graduate students and researchers interested in learning cleanroom procedures and safety. Lectures will focus on theory, simulation, and procedures, while the laboratory will provide safety training and hands on learning of the instruments and procedure used within the ECE Engineering Research Complex Cleanroom. As part of this course various devices will be fabricated and tested such that experience will be gained with each of the instruments in the ECE – Cleanroom.

COURSE OBJECTIVES:
At the completion of this course, each student should be able to do the following:
1. Follow proper gowning procedures for entering a class 1000 cleanroom.
2. Describe activities that deteriorate the cleanliness of a cleanroom.
3. Describe common safety concerns associated with chemicals used in the ECE Cleanroom.
4. Demonstrate proper operation of the ECE Cleanroom systems including:
   - Wafer cleaning
   - Standard lithography process
   - Plasma Enhanced Chemical Vapor Deposition (PECVD)
   - Physical Vapor Deposition (PVD): Sputtering, and thermal evaporation
   - Wet chemical etching (of SiO_2, Si_3N_4, and/or TiN)
   - Reactive Ion Etching (RIE)
   - Thermal oxidization of wafers
5. Fabricate silicon diodes, capacitors, resistors, MOSFETs, and NMOS logic gates.
6. Measure the electrical transport properties of the devices made.
7. Run computer simulations of the processes and devices.

TEXT (Found at the Main Library):

1. Silicon VLSI Technology: Fundamentals, Practice, and Modeling, J.D. Plummer, M.D. Deal, P.B. Griffin, Prentice Hall, (2000).
2. Introduction to Microelectronic Fabrication, 2nd Ed. by Richard C. Jaeger, Volume V in the Modular Series on Solid State Devices, Prentice Hall, New Jersey, (2002).
3. Fundamentals of Microfabrication: The Science of Miniaturization, 3rd Ed. by M. J. Madou, CRC Press, Boca Raton, FL, (2012).
4. Microchip Manufacturing, S. Wolf, Lattice Press, Sunset Beach, CA, (2004).

GRADING:

Homework: 10%
Exam1: 20%
Exam2: 20%
Project Report and Presentation:............................ 25%
Laboratory Reports & Participation: 25%

Homework Policy:

There are 6-7 problem sets throughout the semester. Homework is due at the beginning of class and no late homework is graded. Each student must turn in individual work. There is no restriction on cooperation, discussions, use of other sources for the homework assignments. If a solution to a problem is found in the literature, correct citations to the literature must be provided. All homework scores will be included in the course grade.

Lab Policy:

You are expected to make the scheduled lab times. The instructor will be there at the start of the lab time to let you into the gowning room. Makeup times can be difficult to schedule, but if necessary then work out a convenient time with the instructor to makeup the lab.

A lab report is due one week after you took the lab. You turn in your lab report by uploading it to the D2L website through the assignments folder. The general template for your reports include a cover sheet followed by a brief introduction describing what was done in the lab, followed by a section related to the measurements, notes, and/or reference materials related to the lab. Each lab report will be graded on a 10 point basis, and a template for each lab which includes questions for you to answer within your report will be provided.

Exam Policy:

Two 50-minutes Midterm Exams are held in the classroom during the regularly scheduled class time. Calculator is permitted in the exams unless it has features described on the "Prohibited" list below.

Prohibited:
- Pocket organizers
- Handheld pocket organizers
- Handheld or laptop computers
- Electronic writing pads or pen-input devices
- Calculator built into cell phones or other electronic communication devices
- Calculators with a typewriter keyboard (key in QWERTY format)

Project Report & Presentation:

Graduate students will simulate the processes used for fabrication of one of the devices in the course along with a device simulation for the same device. They will then prepare a report and a presentation for the results

of the simulation along with measured results of the device modeled and a comparison to the expected results.

The final exam period (Monday, December 9, 2019 from 3:00pm – 5:00pm in 1300 Engineering Building) will be used for project presentations.

Approximate Timeline:

	Day	Date	Topics Covered	Labs
1	W	August 28	Introduction – History and Market	Gown Sizing (in class)
	M	September 2	University Holiday (No class)	Lab #1 Safety & 4 point probe
2	W	September 4	Lithographic Process – wafer cleaning	
3	M	September 9	Lithographic Process – oxidation	Lab #2 Clean & PECVD Oxide
4	W	September 11	Lithographic Process – patterning, etching	
5	M	September 16	Lithographic Process – etching	Lab #3 Lithography-Mask1
6	W	September 18	Semiconductor Physics	
7	M	September 23	Semiconductor Physics	Lab #4 Diffusion Doping
8	W	September 25	Semiconductor Physics	
9	M	September 30	Semiconductor Physics	Lab #5 Clean & PECVD Oxide
10	W	October 2	Diffusion & Ion Implantation	
11	M	October 7	Diffusion & Ion Implantation	Lab #6 Pattern & Thin Oxide-Mask2
	W	October 9	Exam 1	
12	M	October 14	Physical Vapor Deposition	Lab #7 Pattern for vias-Mask3
13	W	October 16	Physical Vapor Deposition	
14	M	October 21	Interconnects and Contacts	Lab #8 PVD of Metals
15	W	October 23	Interconnects and Contacts	
16	M	October 28	Device Characterization	Lab #9 Pattern Metals-Mask4
17	W	October 30	Device Characterization	
18	M	November 4	Chemical Vapor Deposition	Lab #10 Device Testing
19	W	November 6	Chemical Vapor Deposition	
20	M	November 11	MEMS	Lab #11 Device Testing
	W	November 13	Exam 2	
21	M	November 18	MEMS	Lab #12 Device Testing
22	W	November 20	Surface Micromachining – laser	
23	M	November 25	Surface Micromachining – laser	No Lab – Thanksgiving Break
24	W	November 27	Packaging & Yield	
25	M	December 2	MOS Process Integration	
	W	December 4	MOS Process Integration	
		December 9	Final Exam Time Period (Student Presentations)	